AMENDMENTS TO THE CLAIMS

Claims 1-16 (Cancelled)

17. (Currently amended) The method of Claim [[16]] 32, wherein the FPGA ~~is~~ programmed to perform steps including ~~performing a portion of a simulation on the programmable device includes:~~

receiving the real and imaginary inputs at first and second inputs of an FFT block via ~~the data path into~~ a pair of gateway in blocks;

coupling [[the]] an output of [[the]] a double delay block to a third input of the FFT block, the third input being adapted to mark data input as valid or invalid;

coupling [[the]] an output of a k=0 block to a fourth input of the FFT block, the fourth input being adapted to control a forward or a reverse transform;

~~providing a real component output from the FFT block; providing an imaginary component output from the FFT block;~~

~~providing a third output from the FFT block adapted to mark the output data as valid or invalid;~~

~~providing a fourth output from the FFT block that is active high on a first output sample in a frame;~~

~~providing a fifth output from the FFT block that is active high when the FFT block can accept data;~~

coupling outputs of ~~the real component output, imaginary component output, third output, fourth output, and fifth output from~~ the FFT block to at least one D flip flop-based registers adapted to provide a signal latency; and

coupling the outputs of the registers to at least one gateway out.

Claims 18-30 (Cancelled)

31. (New) A method of performing a numerical simulation with a CPU and an FPGA, comprising:

using the CPU to perform a numerical simulation including generating input signals and sending the input signals to the FPGA;

using the FPGA to apply a model to the input signals and send results of the model back to the CPU, the FPGA also generating a first output that marks data as valid or invalid, a second output that indicates the first sample of each frame, and a third output that indicates when the model can accept data; and

wherein the CPU uses the results in the numerical simulation and the outputs to maintain data flow with the FPGA.

32. (New) The method of claim 31, wherein the input signals include sine wave functions representing real and imaginary inputs; and wherein the model includes a FFT.

33. (New) The method of claim 32, wherein the FPGA converts the real and imaginary inputs from double point precision to fixed point prior to performing the transform; and wherein the FPGA converts the results of the FFT from fixed point back to double precision prior to sending the results back to the CPU.

34. (New) The method of claim 32, wherein the CPU performs a numerical simulation of a radar system.

35. (New) Apparatus comprising:

a CPU programmed to perform a numerical simulation of sine wave functions representing real and imaginary inputs; and

an FPGA programmed to perform an FFT on the inputs and send results of the FFT back to the CPU, the FPGA also generating a first output that marks data as valid or invalid, a second output that indicates the first sample of each frame, and a third output that indicates when the FFT can accept data; and

the CPU using the results in the numerical simulation and the outputs to maintain data flow with the FPGA.

36. (New) The apparatus of claim 35, wherein the FPGA converts the real and imaginary inputs from double point precision to fixed point prior to performing the transform; and wherein the FPGA converts the results of the FFT from fixed point back to double precision prior to sending the results back to the CPU.

37. (New) The apparatus of claim 35, wherein the CPU performs a numerical simulation of a radar system.